REMARKS/ARGUMENTS

Applicants received the Office Action dated March 17, 2004, in which the Examiner: (1) rejected claims 1, 3-8, 10-12, 14-17 and 19-24 as obvious in view of U.S. Pat. App. Pub. No. 20020002262 ("Olarig") and U.S. Patent No. 6,298,384 ("Sudo"); and (2) rejected claims 2, 13 and 18 as obvious in view of Olarig, Sudo and U.S. Pat. App. Pub. No. 20020091905 ("Geiger"). In this Response, Applicants amends claims 1, 2, 8, 10, 15 and 16. Also, claims 25 and 26 have been added. No claims have been canceled. Based on the amendments and arguments contained herein, Applicants respectfully requests reconsideration and allowance of the pending claims.

Rejections Under 35 USC § 103

To reject a claim under 35 USC § 103, the examiner must establish prima facie obviousness. One factor required to establish prima facie obviousness of a claimed invention is that all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). See MPEP 2143.03. Applicant traverses the §103 rejections and respectfully submits that the examiner has not established a prima facie case of obviousness because the cited art does not teach or suggest all the claim limitations.

Claim 1

Claim 1 was amended, in part, to replace the phrase "a plurality of busses" with "a first group of bus lines" and "a second group of bus lines." Amended claim 1, in part, requires "each group of bus lines includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines." None of the references cited by the Examiner teaches or suggests these limitations. The Examiner recognizes that Olarig does not teach unidirectional bit lines and cites Sudo as teaching unidirectional bit lines. While Sudo does teach unidirectional data transfer, Sudo does not teach or suggest bus lines having "two unidirectional bit lines for each data bit" as required in claim 1.

Furthermore, none of the references cited by the Examiner teaches or suggest "bus bridges [that] include a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1. The Examiner seems to argue that a multiplexer 720 shown in

Olarig's Figure 10 is equivalent to Applicants' claimed "bus bridge" (see Office Action, page 3, paragraph 1). However, Olarig specifically teaches that the multiplexer 720 is part of serial presence detect logic that "converts Parallel Presence Detect bits into Serial Presence Detect protocol" (see paragraph [0073]). Olarig further teaches that the logic (including the multiplexer 720) of Figure 10 is only used because some older DIMMs do not provide the presence detect value in a serial format (see paragraphs [0073] – [0077]). Olarig does not teach "bus bridges [that] include a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1.

Sudo teaches a switch 13 that includes multiplexers 13A, 13B and 13C. Specifically, the multiplexer 13A outputs either an input provided to the processing module 10, an output from a shared memory 15 or an output from a CPU 14 of the processing module 10 to an output connector 12 of the processing module 10. The multiplexer 13B outputs either the input provided to the processing module 10 or the output of the CPU 14 of the processing module 10 to the shared memory 15. The multiplexer 13C outputs either the input provided to the processing module 10 or the output from the shared memory 15 to the CPU 14 of the processing module 10. However, the multiplexers 13B and 13C do not "[select] from three other incoming bit lines" as required in claim 1. For at least these reasons, Applicants submit that claim 1 and all claims that depend from claim 1 are allowable.

Claim 11

Claim 11, in part, requires "local busses [that] each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit." For at least the reasons described previously, with respect to claim 1, none of the art cited by the Examiner teaches or suggests that this limitation. For at least this reason, Applicants submit that claim 11 and all claims that depend from claim 11 are allowable.

Claim 15

Amended claim 15, in part, requires "a cross-bus for transferring data among the plurality of local bus groups, wherein said cross-bus is coupled to each of the plurality of local bus groups by a bridge means that includes bi-directional data channel bridges and uni-directional address channel

bridges." The Examiner seems to equate, at least, the multiplexer 720 shown in Fig. 10 of Olarig with Applicant's claimed "bus bridge" (see Office Action, page 2, second bullet point). However, as described previously, the multiplexer 720 only functions to convert parallel presence detect bits into serial presence detect protocol. Neither the multiplexer 720, the memory controller 200a, nor the memory personality modules 300a-300d taught in Olarig includes "bi-directional data channel bridges and uni-directional address channel bridges" as required in claim 15.

Further, while Sudo does teach unidirectional data lines, neither the switch 13, the switch controller 16, nor the connectors 11, 12 include both "bi-directional data channel bridges and uni-directional address channel bridges" as required in claim 15. For at least these reasons, Applicants submit that claim 15 is allowable.

Claim 16

Amended Claim 16, in part, requires "one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection and wherein the local intersect busses are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses." As described previously, with respect to claim 1, none of the art cited by the Examiner teaches or suggests "four multiplexers at each intersection" as required in claim 16. Furthermore, none of the art cited by the Examiner teaches or suggests "local intersect busses [that] are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses" as required in claim 16.

Furthermore, claim 16 requires "local memory busses that each include two unidirectional bit lines for each data bit" and "local intersect busses [that] each include two unidirectional bit lines for each data bit." As described previously, with respect to claim 1, none of the art cited by the Examiner teaches or suggests this limitation. For at least these reasons, Applicants submit that claim 16 and all claims that depend from claim 16 are allowable.

New Claims

Claim 25, in part, requires "a set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable

between the sets of bus lines via the cross-bus lines, wherein the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable."

None of the references cited by the Examiner teaches or suggests "cross-bus lines [that] are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable." For at least this reason, Applicants submit that claim 25 and all claims that depend from claim 25 are allowable.

REMARKS

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicant submits that this response constitutes a complete response to all of the issues raised in the office action of March 17, 2004. Applicants have responded to the various rejections under 35 USC §103. In view of the foregoing amendments and remarks, Applicants submit that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned if a telephone interview might prove helpful in resolving this application.

If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Corporation Deposit Account Number 12-2252/5201-20400/DJK.

Respectfully submitted,

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